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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/682,188	08/02/2001	Makoto Ueda	JP920000046US1	5265

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F. CHAU & ASSOCIATES, LLC
130 WOODBURY ROAD
WOODBURY, NY 11797

EXAMINER	
TANG, KENNETH	
ART UNIT	**PAPER NUMBER**
2195	

DATE MAILED: 10/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/682,188	UEDA, MAKOTO	
	Examiner	Art Unit	
	Kenneth Tang	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to the Amendment filed on 6/24/05. Applicant's arguments have been fully considered but are moot in view of the new grounds of rejections.

2. Claims 1-21 are presented for examination.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable by Pong (US 2002/0053004 A1) in view of Hunter et al. (hereinafter Hunter) (US 6,665,699 B1).

4. As to claim 1, Pong teaches in multiprocessing, which is performed by using a module including a cache memory and a plurality of processors sharing the cache memory (shared cache) *([0064], Fig. 4 and 5)*, a method of allocating a task to each processor comprising the steps of:

monitoring (track) access conditions (state information) of respective tasks to data shared among cache memories (requesting access to shared cache) in the processor modules *(page 1, [0003]-[0004], [0013])*; and

allocating tasks that make frequent accesses to the same shared data to processors in the same module (buffering most frequently accessed data blocks), on the basis of said access conditions (state information) *(page 6, claim 17, page 1, [0003]-[0004], [0013]).*

Pong fails to explicitly teaches using a single module that includes a plurality of processors and a shared cache (see Fig. 4 and 5) but fails to explicitly teach having a plurality of modules. However, Hunter teaches that it is well known in the art to have a plurality of modules wherein each module includes a plurality of processors with a shared cache memory (Fig. 3). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Pong with Hunter in order to increase memory capacity of the cache and to increase system throughput *(col. 1, lines 44-64)*.

5. Claims 2-5, 9-12, and 15-18, and 21are rejected under 35 U.S.C. 103(a) as being unpatentable over Pong (US 2002/0053004 A1) in view of Hunter et al. (hereinafter Hunter) (US 6,665,699 B1), and further in view of Kaneko et al. (hereinafter Kaneko) (US 5,349,656).

6. As to claim 2, Pong teaches wherein said step of monitoring access conditions comprises the substeps of:

detecting ("snooping") an update (write update) to the shared data stored in a cache memory in one of the processor modules, said update causing an invalidation (write invalidation) of the shared data stored in the cache memories in the other processor modules *(page 1, [0004], page 4, [0048]-[0049])*; and

storing tasks that caused said invalidation, and an address of the updated data, and the number of invalidations of the same data by the same task *(page 1, [0005], page 4, [0057])*, and Pong teaches keeping track of the number of data accesses and to determine if they are frequent accesses but fails to explicitly teach allocating tasks where the tasks are classified into groups and allocating to the processor module by the group. However, Kaneko teaches classifying and grouping tasks into groups based on whether they share common data for allocation *(col. 9, lines 30-37)*. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Kaneko's teaching of allocating tasks where the tasks are classified into groups and allocating to the processor module by the group to the existing system of Pong because this increases efficiency by allocating tasks that are similarly grouped provides execution with the highest buffer storage effect *(col. 9, lines 30-37)*. Kaneko also teaches that tasks have associated with it identification information (task identifier) *(Fig. 4B)*.

7. As to claim 3, it is rejected for the same reasons as stated in the rejection of claim 2. In addition, Pong teaches monitoring access conditions of respective tasks to the invalidated data, and said step of allocating tasks comprises *(page 1, [0003]-[0004], [0013])*.

8. As to claim 4, Pong teaches wherein said substep of monitoring access conditions comprises detecting an access to the invalidated data *(page 1, [0004], page 4, [0048]-[0049])*; and storing an address of the invalidated data, identification information of a task that accessed the invalidated data, and the number of accesses to the same shared data by the same task *(page 1, [0005], page 4, [0057])*.

9. As to claim 5, Pong teaches wherein said detecting an access to the invalidated data comprises detecting an invalidation of data *(page 1, [0004], page 4, [0048]-[0049])*; storing an address of the invalidated data *(page 1, [0005], page 4, [0057])*; detecting a cache miss *(page 5, see claim 7)*; comparing an address of the data that caused the cache miss with the stored address of the invalidated data *(page 1, [0005], page page 3, [0033])*.

10. As to claim 9, it is rejected for the same reasons as stated in the rejection of claim 1. In addition, Pong teaches a memory controller (130) which acts as a detector for detecting accesses by respective tasks to data shared among cache memories (116 and 118) in the processor modules (102 and 104) interconnected with a storage device (110) *(see Fig 1)*. Pong fails to explicitly teach having identification information being associated with tasks. However, Kaneko teaches having task identifiers for a task control block. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the feature of task identifiers associated with the task because this would allow for control of the task control data blocks *(col. 10, lines 22-27)*.

11. As to claim 10, it is rejected for the same reasons as stated in the rejection of claim 2.

12. As to claim 11, Pong teaches wherein said detector for detecting accesses comprises a first device for detecting ("snooping") and storing an update (write update) to the shared data stored in one of a plurality of cache memories (Fig. 1, 116 and 118), said update causing an

invalidation (write invalidation) of the shared data stored in the other cache memories *(page 4, [0048]-[0049])*; and an access detector (memory controller) for detecting accesses to the invalidated data by respective tasks (see Fig. 1, 130).

13. As to claim 12, Pong teaches wherein said detecting an access to the invalidated data comprises detecting an invalidation of data *(page 1, [0004], page 4, [0048]-[0049])*; storing an address of the invalidated data *(page 1, [0005], page 4, [0057])*; detecting a cache miss *(page 5, see claim 7)*; comparing an address of the data that caused the cache miss with the stored address of the invalidated data *(page 1, [0005], page page 3, [0033])*.

14. As to claims 15-18, they are rejected for the same reasons as stated in the rejection of claims 9-12.

15. As to claim 21, it is rejected for the same reasons as stated in the rejection of claim 9.

16. **Claims 6-8, 13-14, and 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pong (US 2002/0053004 A1) in view of Hunter et al. (hereinafter Hunter) (US 6,665,699 B1), in view of Kaneko et al. (hereinafter Kaneko) (US 5,349,656), and further in view of Barajas et al. (hereinafter Barajas) (US 5,598,551).**

17. As to claim 6, Pong and Kaneko fails to explicitly teach making a request for allocation of tasks to an operating system performing multiprocessing, when the total number of said stored invalidations or said accesses exceeds a predetermined value. However, Barajas teaches requesting and making an allocation invalidation operations when exceeding a predetermined value (two clock cycles) *(col. 12, lines 56-60)*. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the feature of making a request for allocation of tasks to an operating system performing multiprocessing, when the total number of said stored invalidations or said accesses exceeds a predetermined value to the existing shared memory multi-processing system with caches in order to minimize delays in processor access to cache memory *(col. 13, lines 40-45)*.

18. As to claim 7-8, 13-14, and 19-20, they are rejected for the same reasons as stated in the rejection of claim 6.

Response to Arguments

19. Applicant's arguments have been fully considered but are now moot in view of the new grounds of rejections.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kenneth Tang whose telephone number is (571) 272-3772. The examiner can normally be reached on 8:30AM - 6:00PM, Every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kt
10/2/05

MENG-AL T. AN
SUPERVISORY PATENT EXAMINER